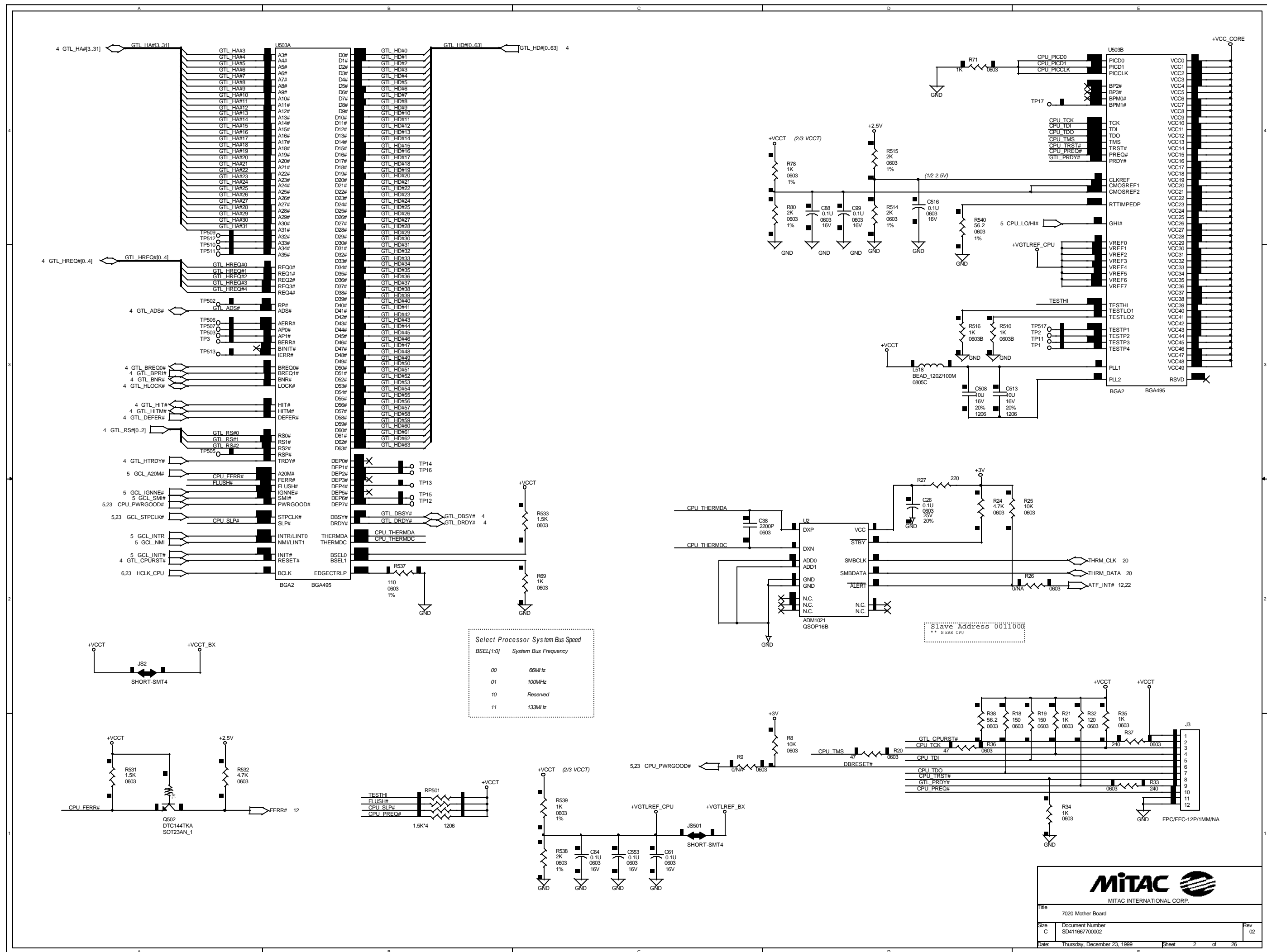
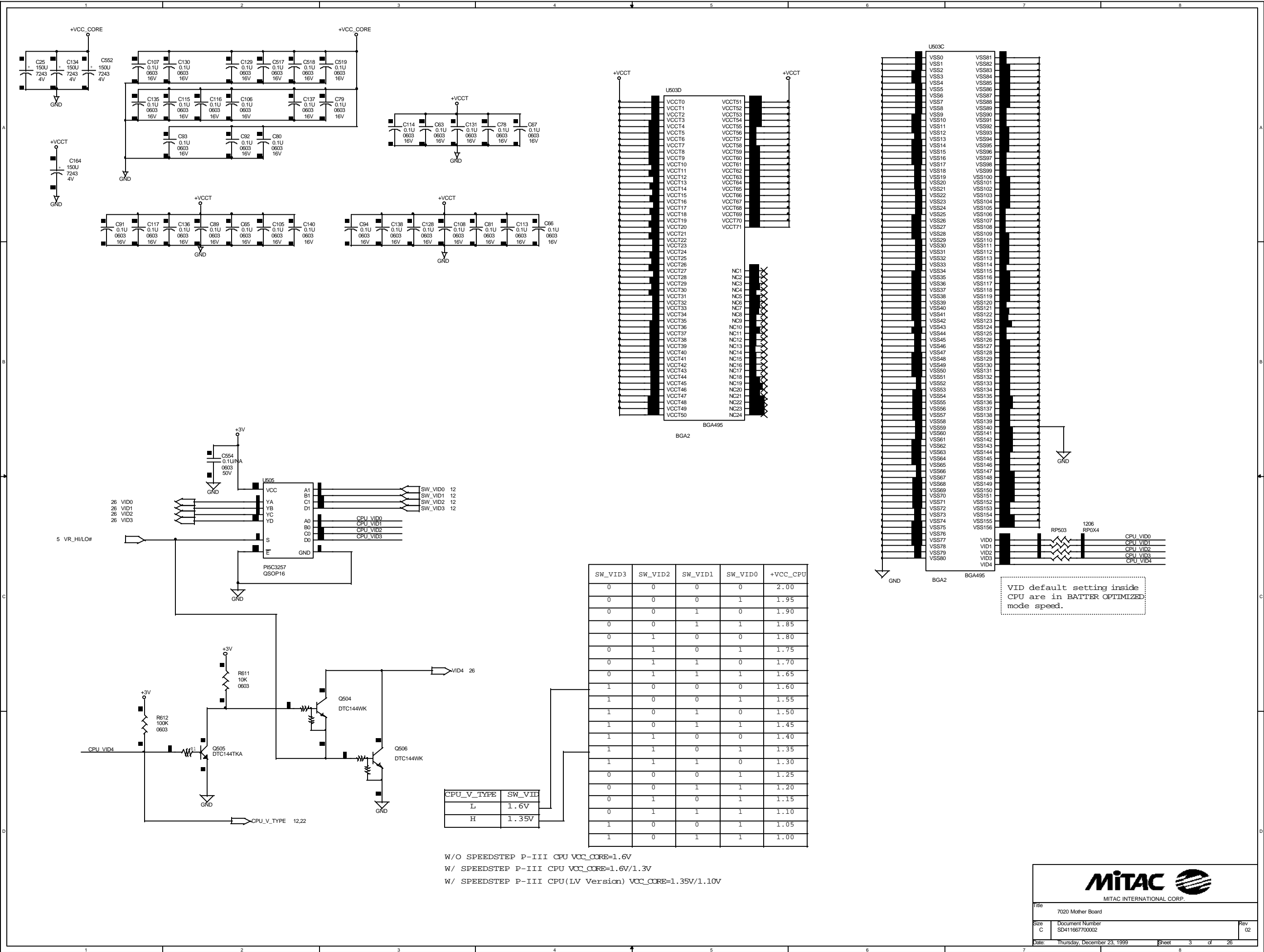
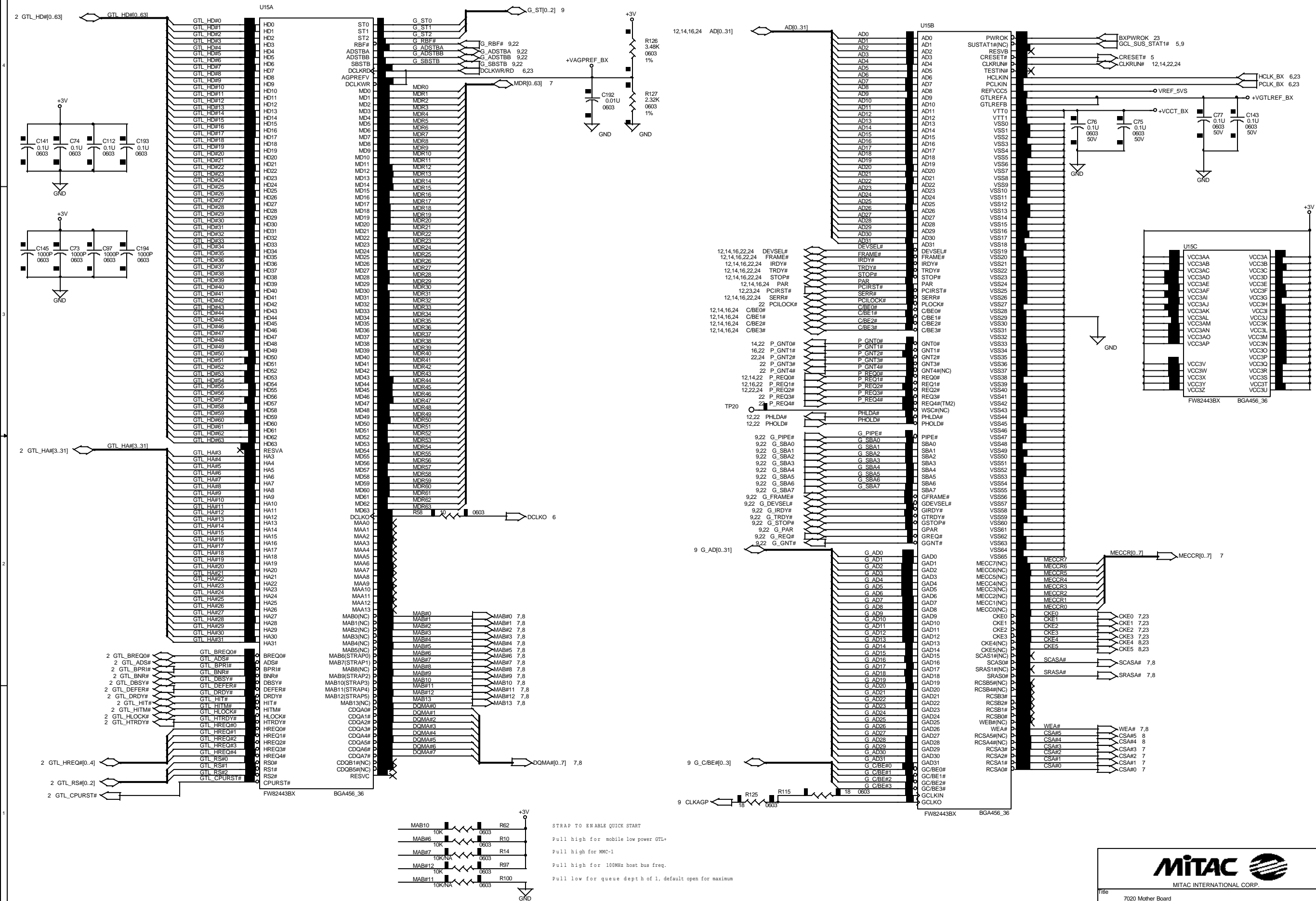


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|   |   |   |   |   |   | REV | DESCRIPTION OF CHANGE   | ECR  |           |
|   |   |   |   |   |   | R00 | uPGA2 with GEYSERVILLE technology   |      | 9/14 '99  |
|   |   |   |   |   |   | R01 | 1. Modify the CPU CORE voltage switching P.3 circuit.<br>2. Correcting BX Strapping Option circuit. P.4<br>3. Correcting parallel port pull-high P.19 circuit.<br>4. Correcting audio SPK-OFF circuit. P.18 |      | 10/20 '99 |
|   |   |   |   |   |   | R02 | 1. Correcting the mistake made by CAPTURE P.26 V.9.0 that make VCC_CORE voltage output fail.  |      | 11/1 '99  |
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## 440BX

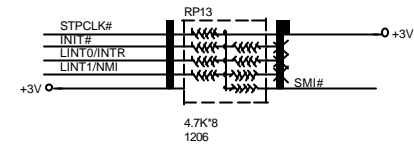


## BX Strapping Option

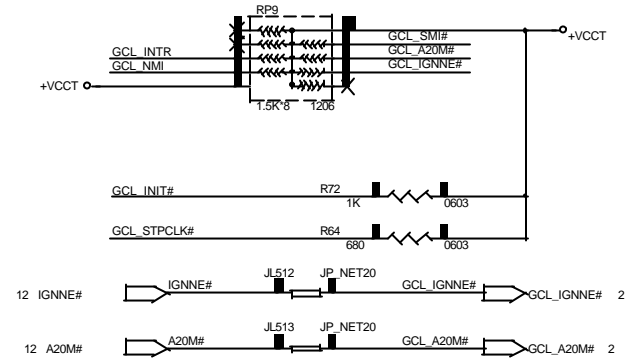


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| Title             |                             |       |         |
| 7020 Mother Board |                             |       |         |
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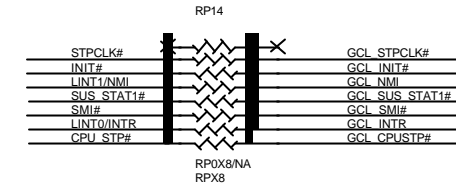
W/GEYSERVILLE MOUNTED THIS RESISTOR ARRAY



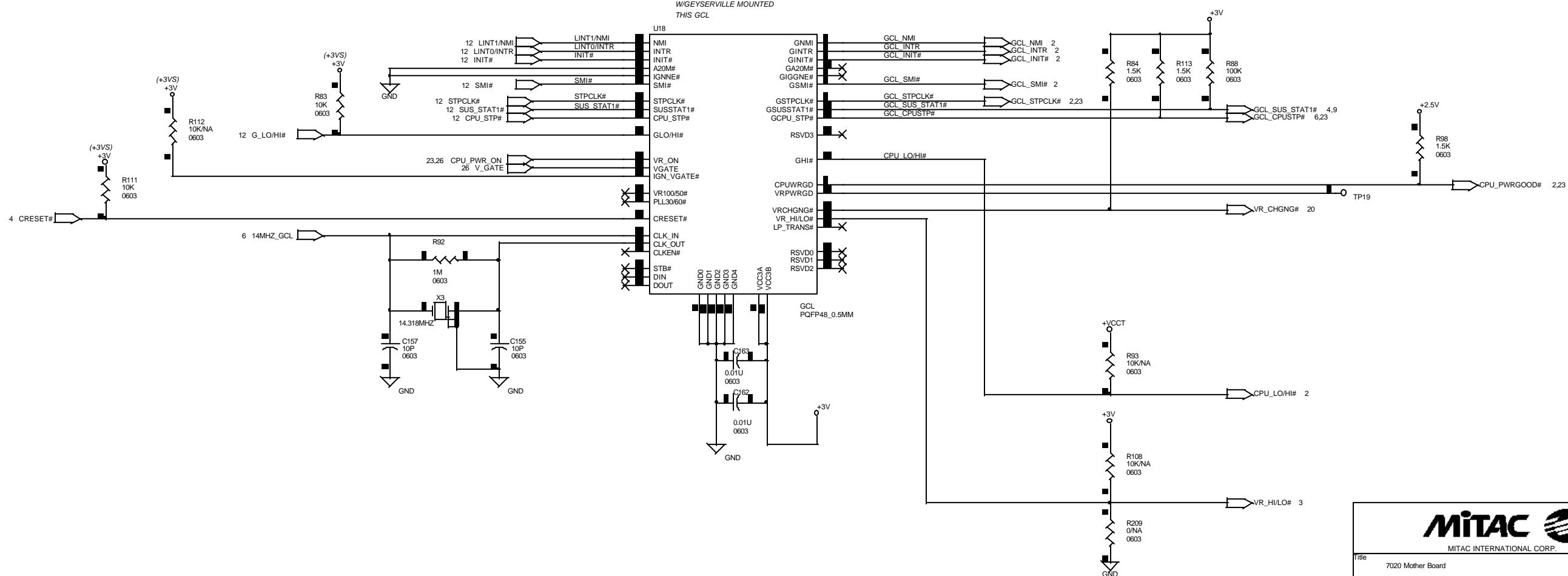
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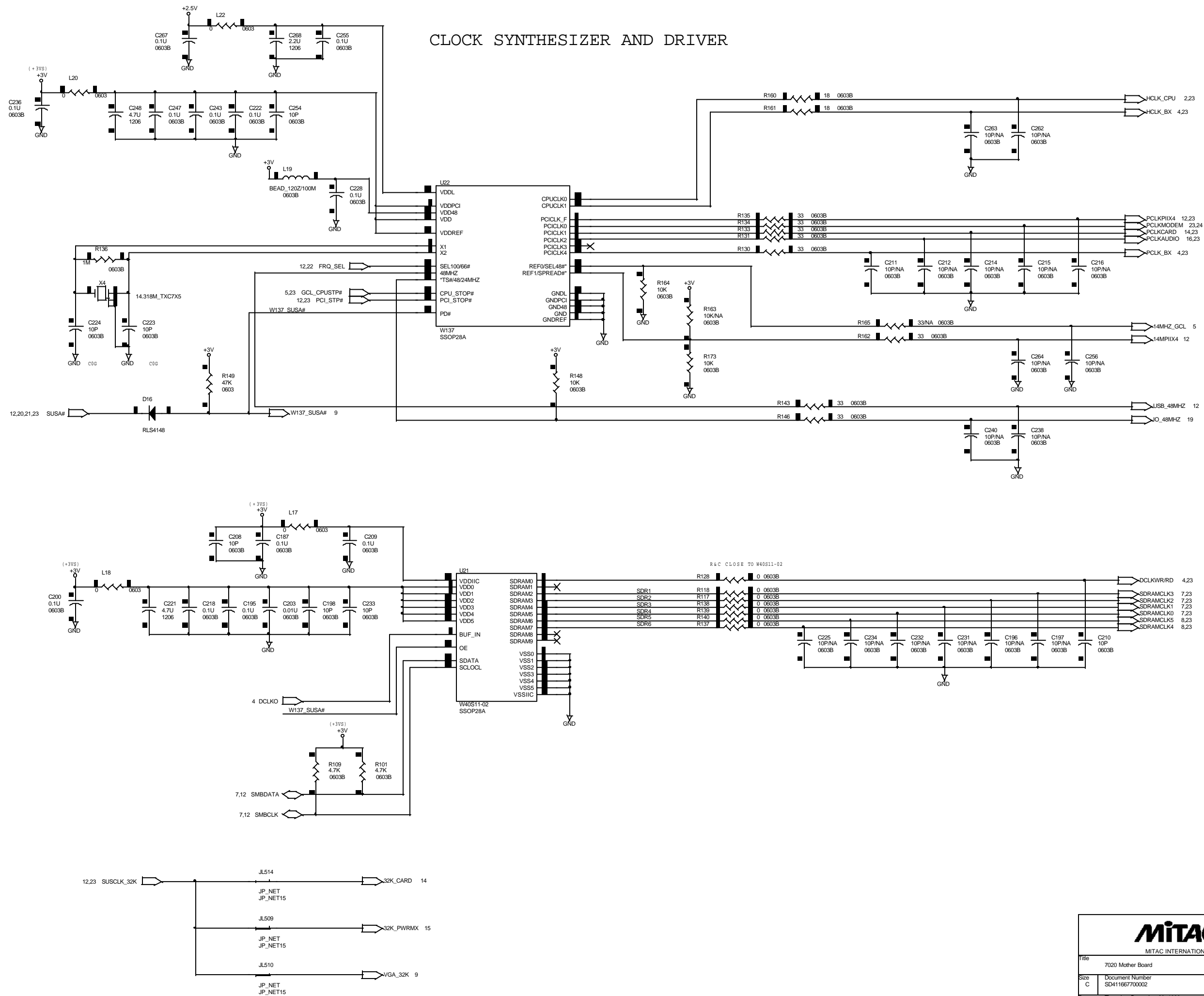
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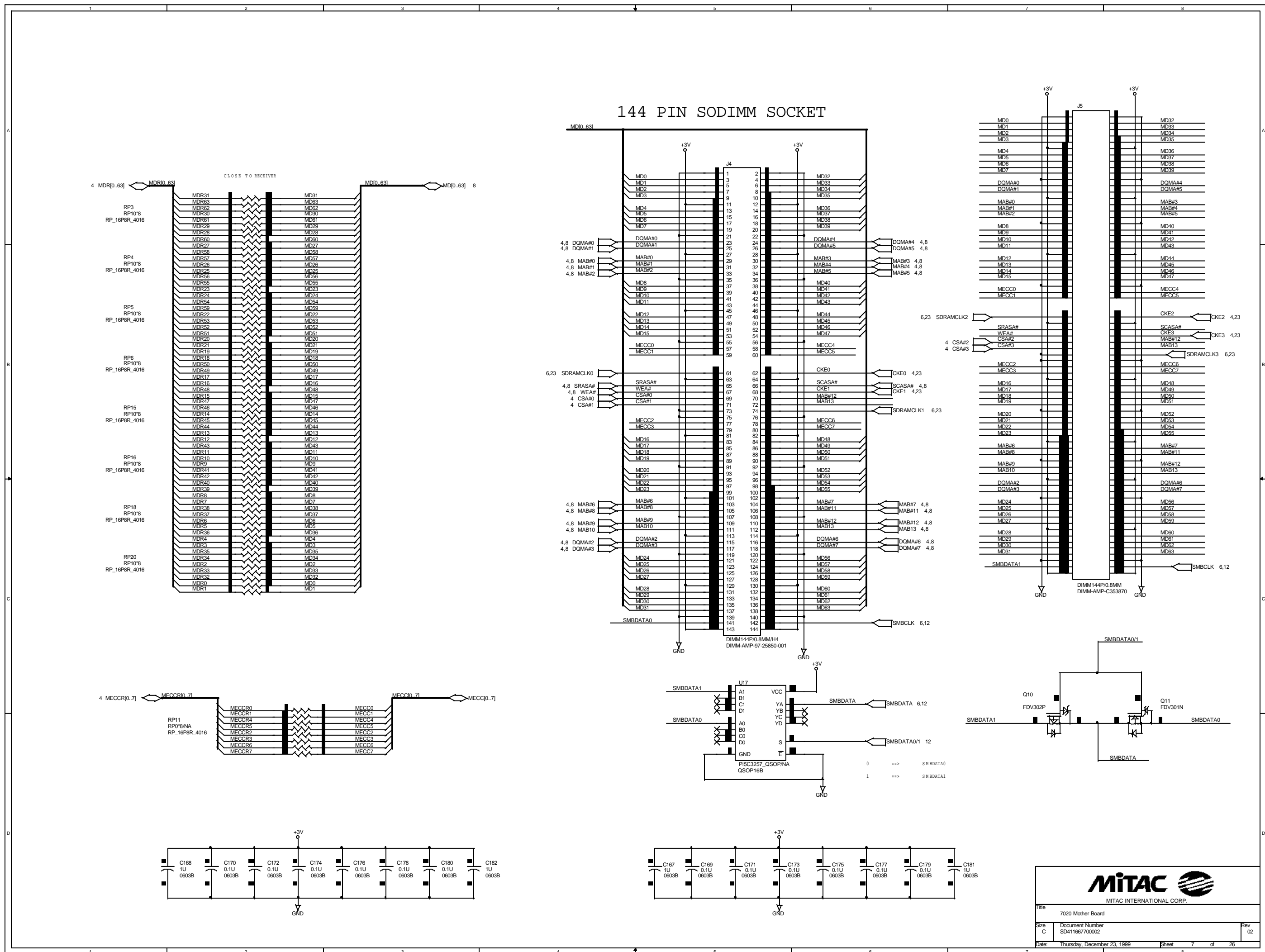


W/GEYSERVILLE MOUNTED THIS GCL



# CLOCK SYNTHESIZER AND DRIVER



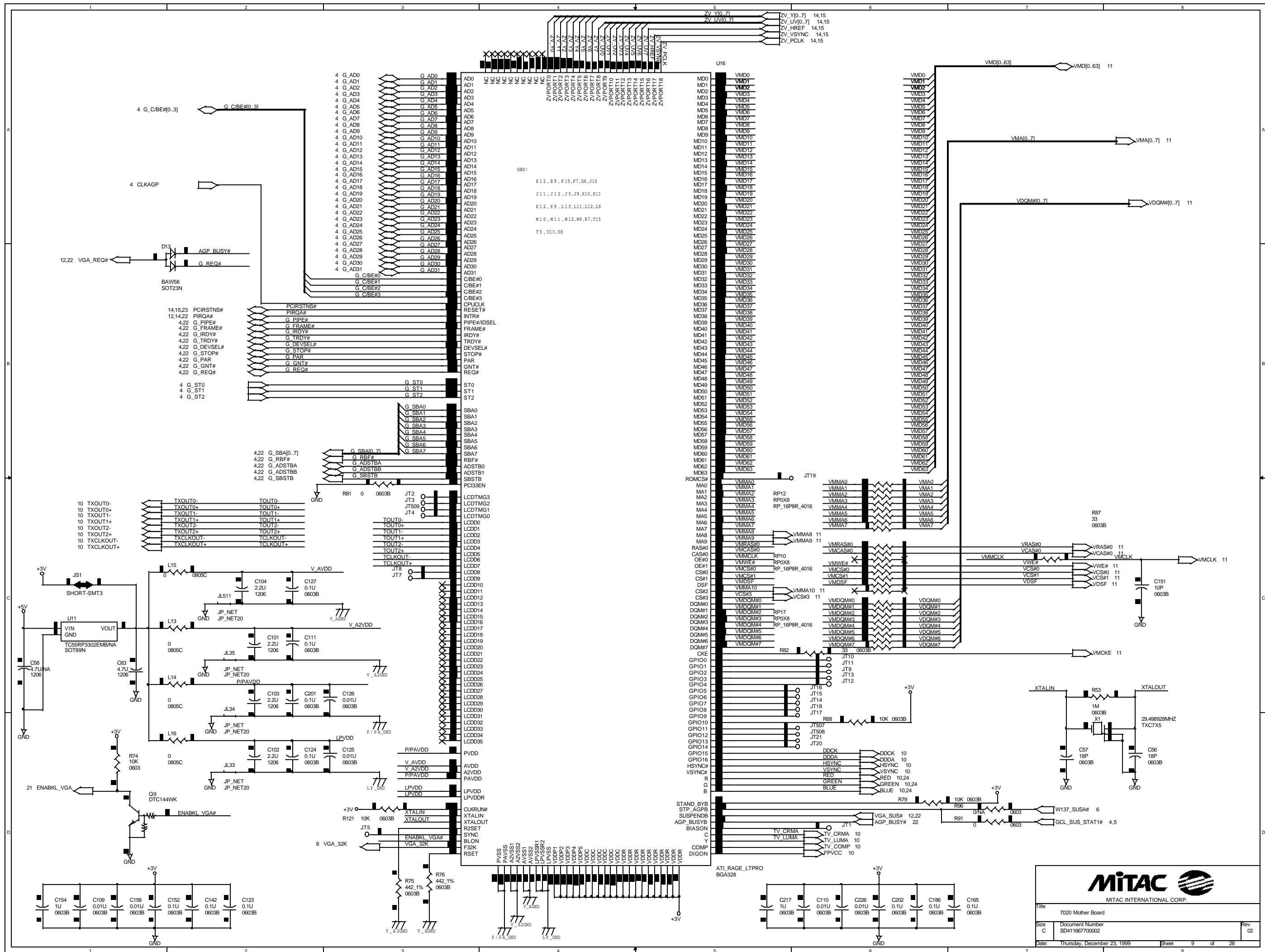


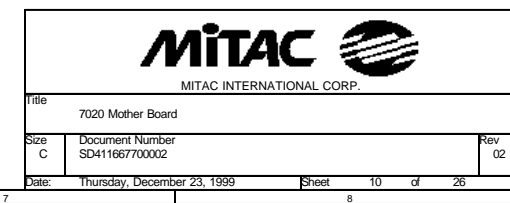
1M X 16 BITS X 4 BANK X 4 = 32M BYTES



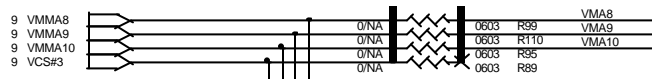
Sheet 8 of 26



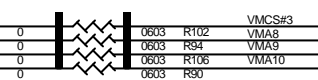




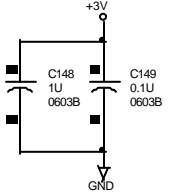
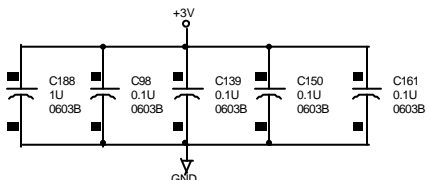
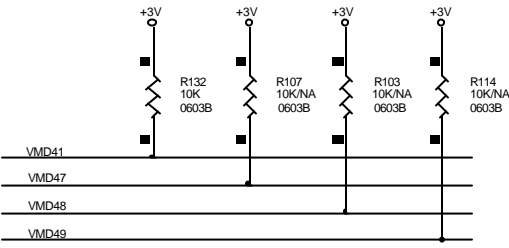
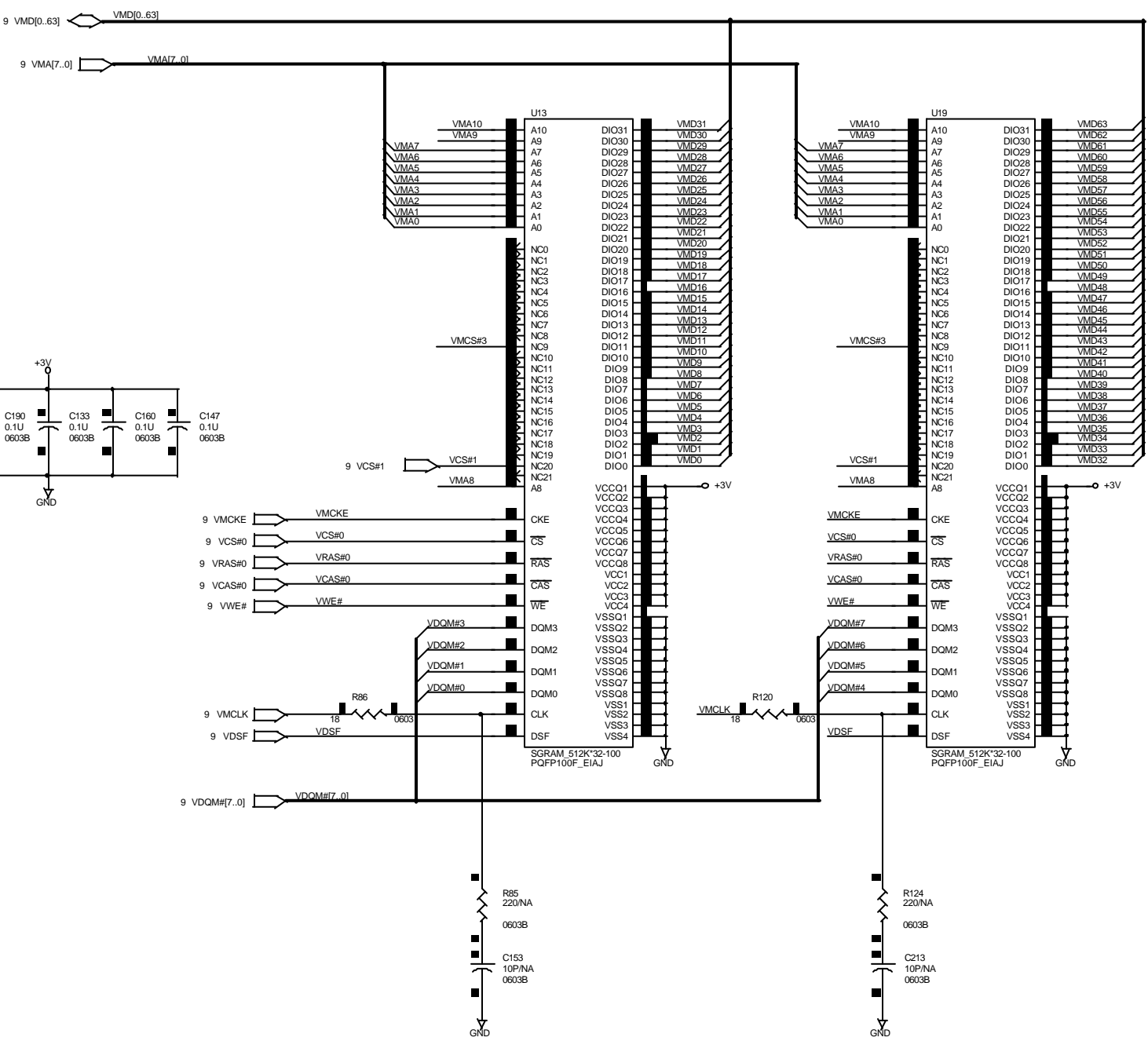
FOR ETRONTECH 8MB SGRAM



FOR SAMSUNG 8MB SGRAM

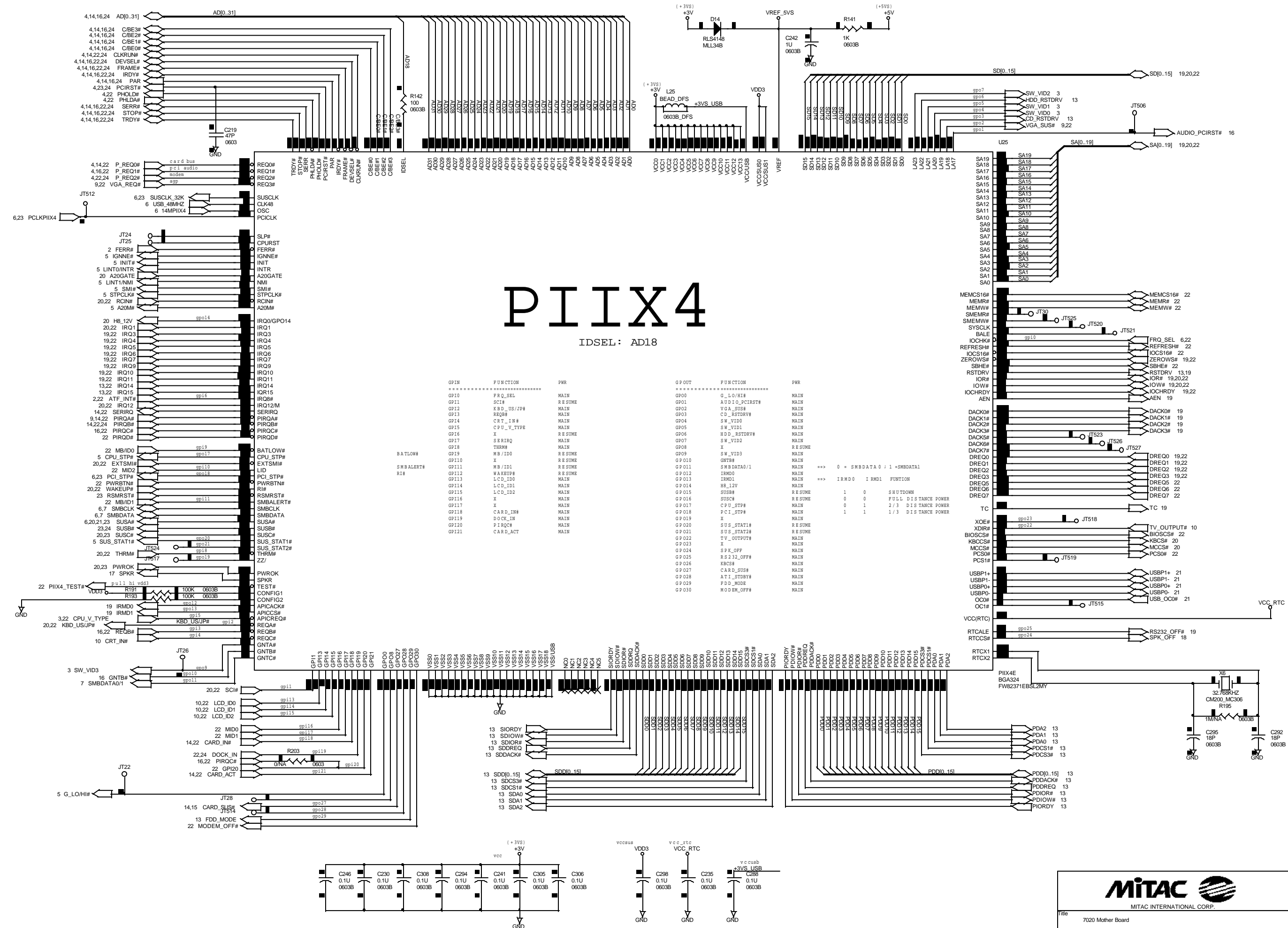


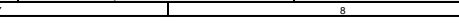
| ATI PIN NAME (VGA) | ETRON (256K*32*2)    | SAMSUNG (256K*32*2) |
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| MA8                | VMA8 (PIN30)         | VMA10 (PIN45)       |
| MA9                | VMA9 (PIN51)         | VMA9 (PIN30)        |
| MA10 (CS#2)        | VMA10 (CS#2) (PIN29) | VMA8 (CS#2) (PIN51) |
| CS#3               | NC                   | BA (PIN29)          |

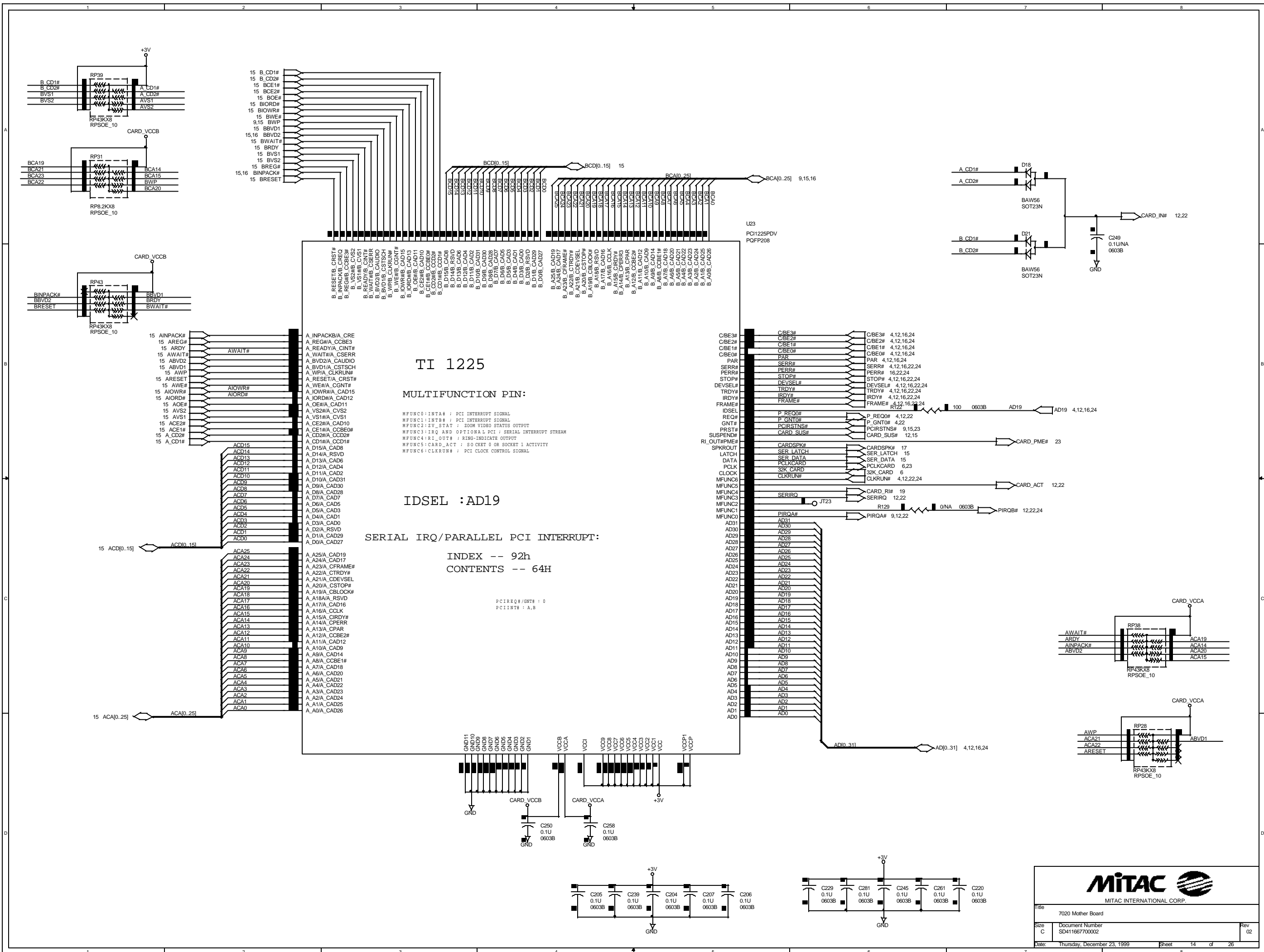


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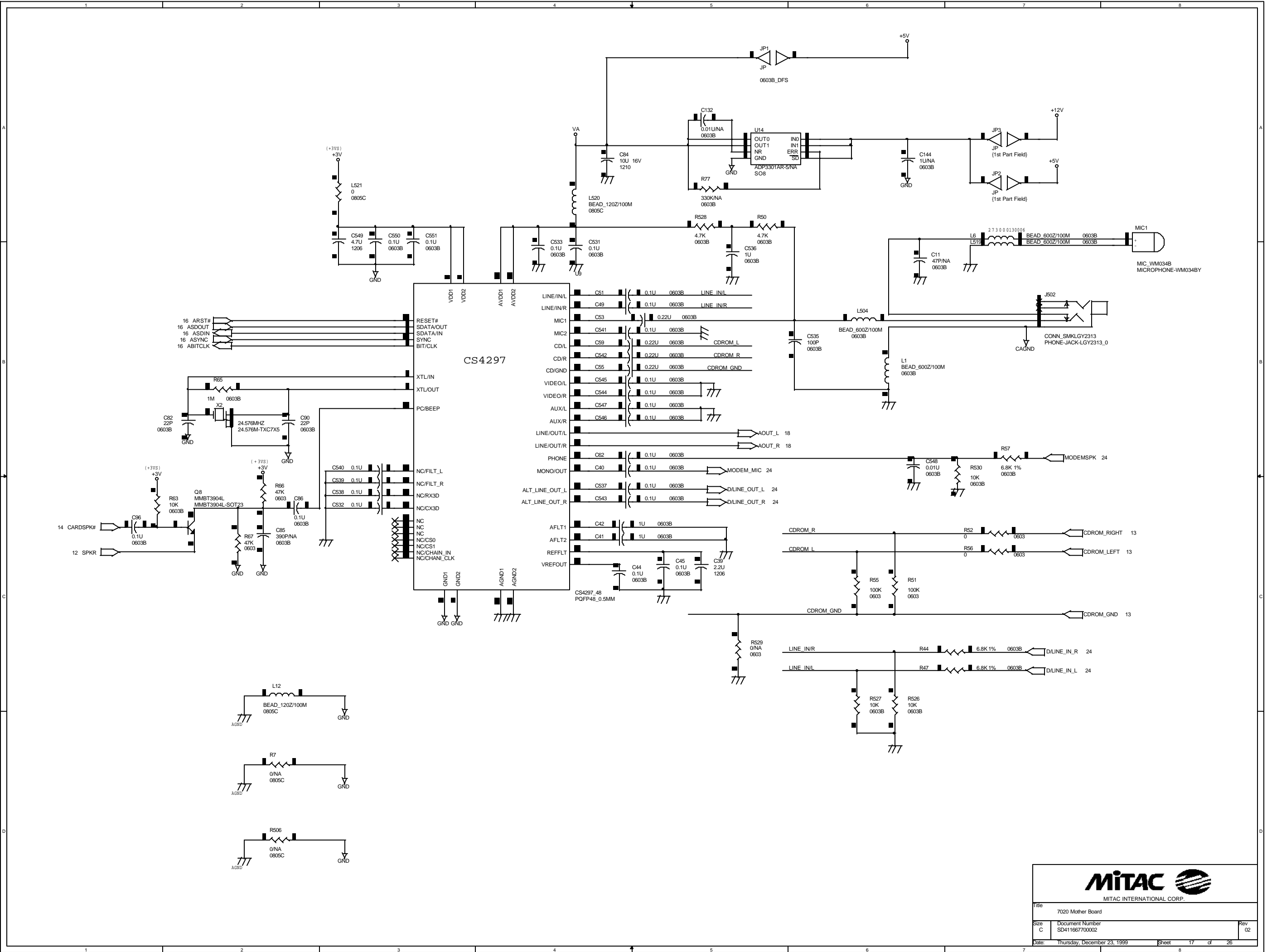




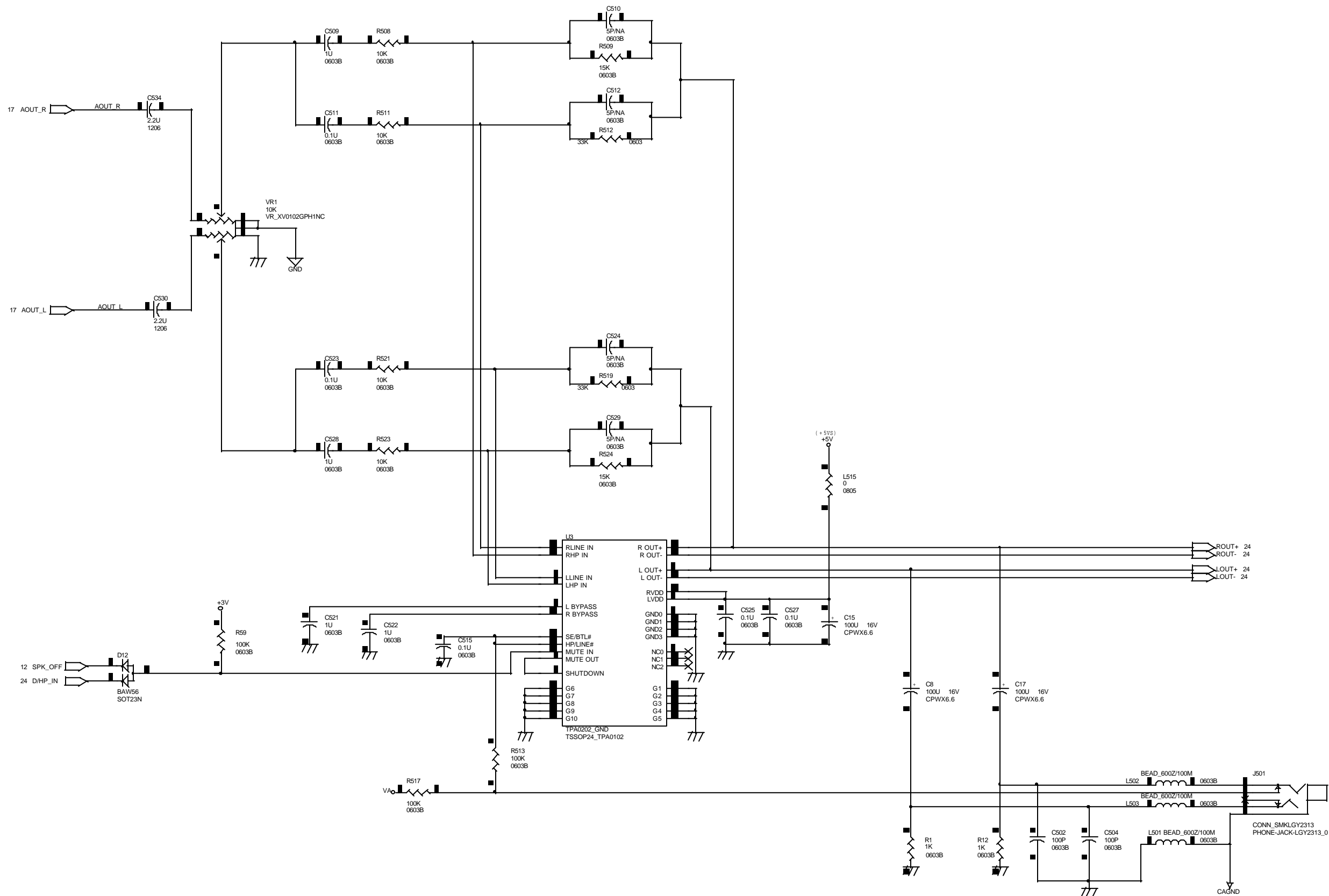




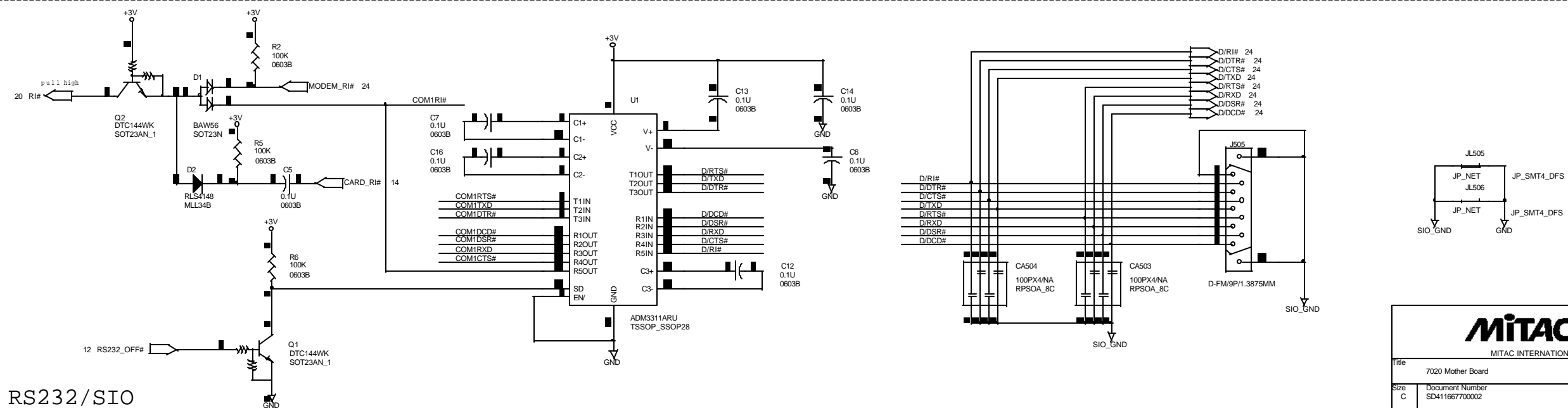


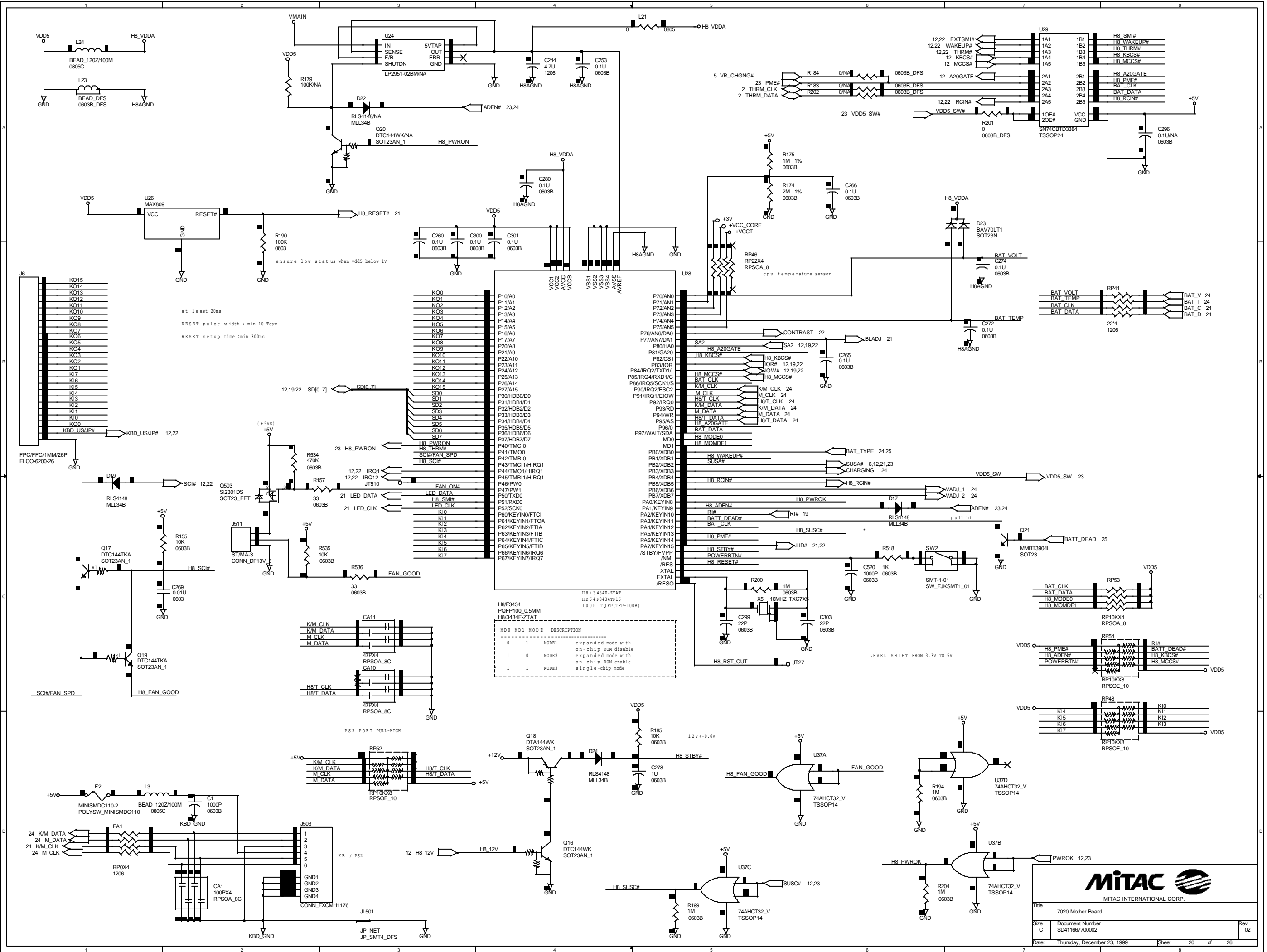


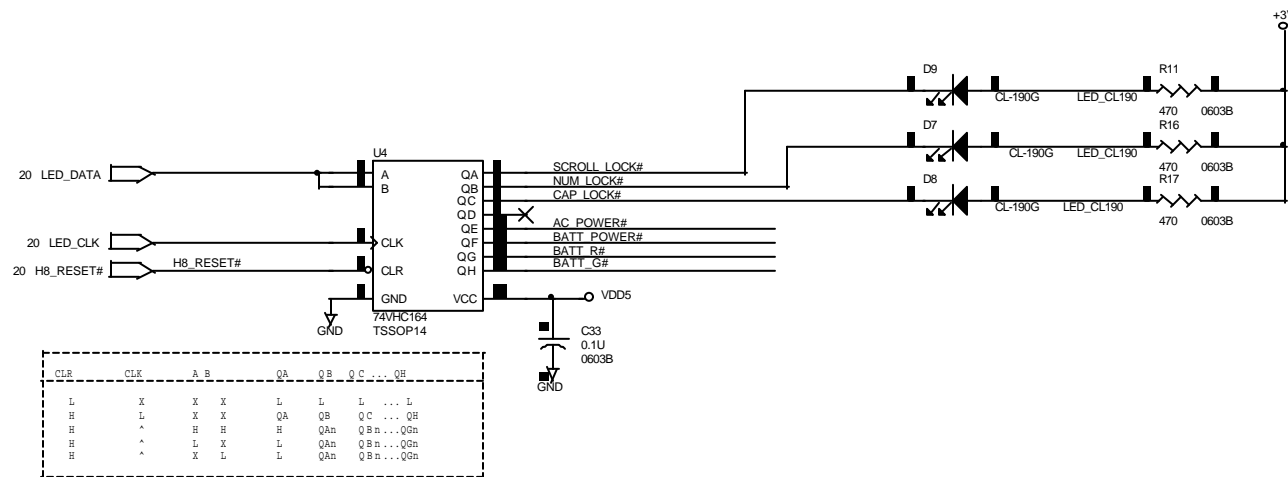
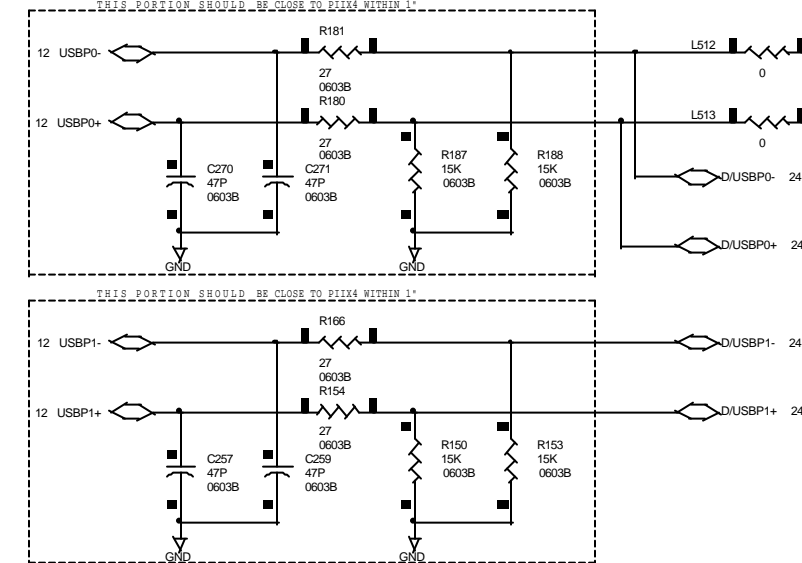
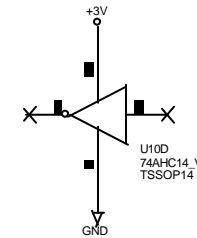
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|-------|-----------------|-----|-----------------------------|
| Title |                 |     | 7020 Mother Board           |
| Size  | Document Number | Rev |                             |
| C     | SD411667700002  | 02  |                             |
| Date: |                 |     | Thursday, December 23, 1999 |
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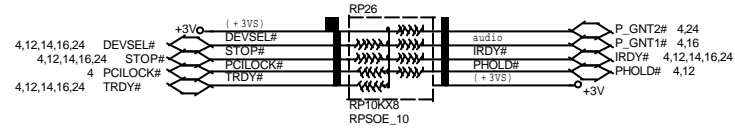
```
CFG0=LOW (DEFAULT):          16 BIT ADDRESS DECODE
CFG1=HIGH (10K PULL-HIGH):    11-BIT ADDRESS/COM2
```



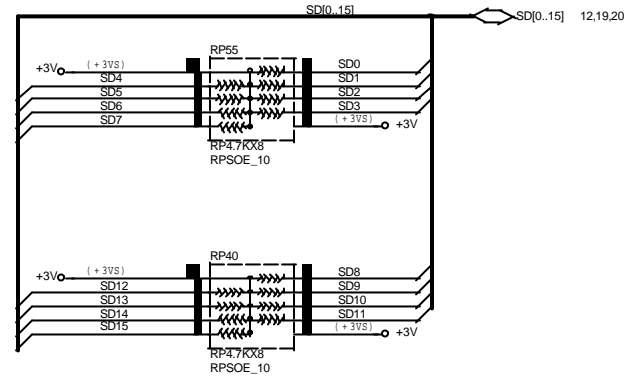




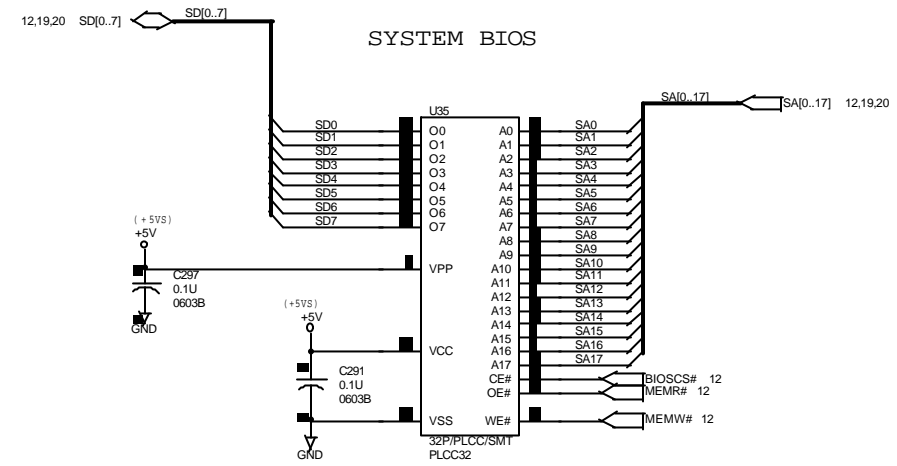
## PCI PULL HIGH



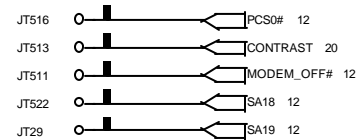
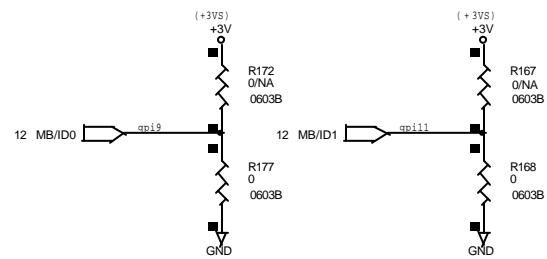
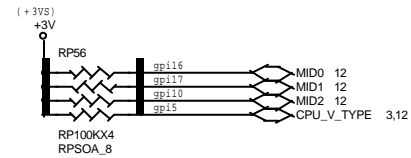
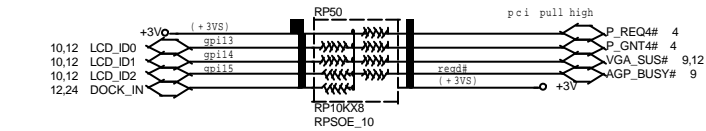
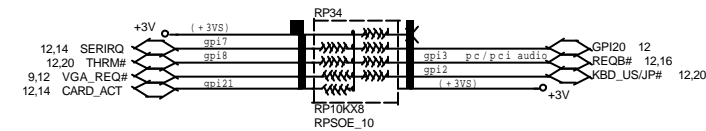
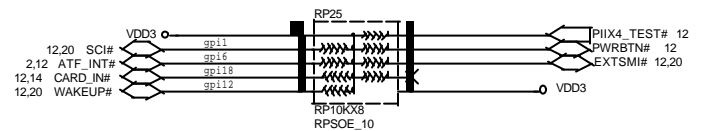
## ISA PULL HIGH



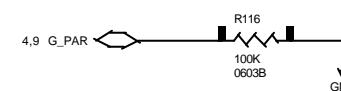
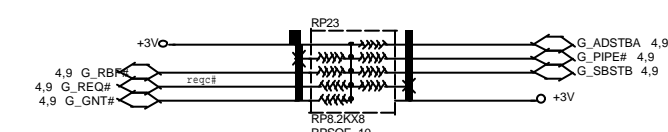
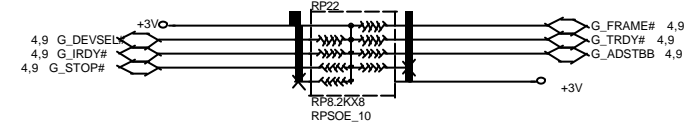
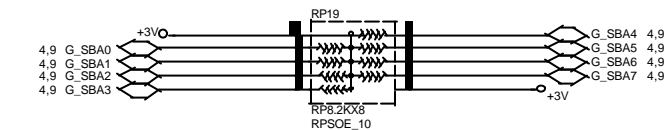
## SYSTEM BIOS



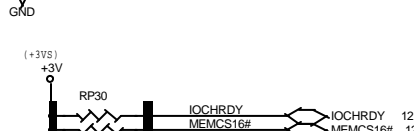
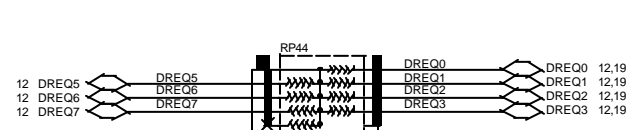
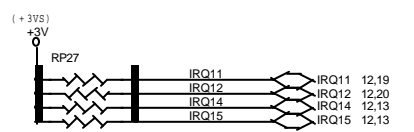
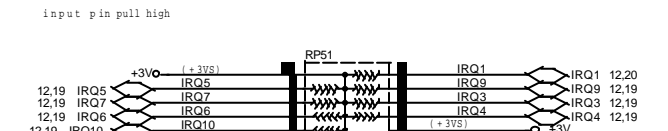
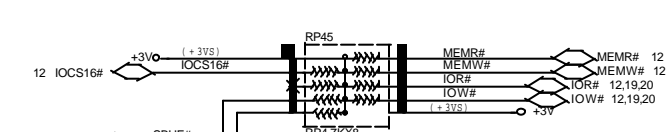
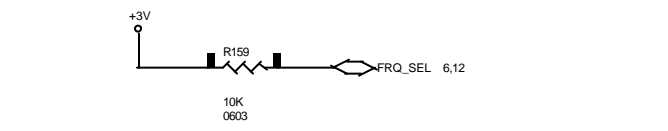
## GPIN PULL HIGH



## AGP PULL HIGH



## PIIX4/AGP PULL HIGH



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